**BCHMS-32 Pipeline Conclusion and References**

**Conclusion**

The BCHMS-32 datapath effectively balances simplicity, performance, and extensibility for low-power health monitoring devices. Through the 5-stage RISC pipeline (IF, ID, EX, MEM, WB), the design achieves predictable timing and efficient instruction throughput while remaining hardware-feasible for embedded contexts.

**Pipeline hazards are mitigated as follows:**  
• **Data hazards** are resolved using forwarding paths (EX/MEM → EX, MEM/WB → EX) and a hazard detection unit that inserts a single-cycle stall on load-use cases.  
• **Control hazards** are minimized with early branch resolution in the ID stage and optional branch prediction for performance-critical applications.  
• **Structural hazards** are avoided by using separate instruction/data memories and distinct integer and floating-point register files.  
• **Floating-point dependencies** are managed via scoreboarding or pipelined FPU forwarding depending on resource constraints.

These optimizations maintain smooth pipeline flow, reduce stall cycles, and ensure real-time signal processing for sensor data. The overall architecture provides a clean and scalable foundation for embedded health-monitoring applications requiring both integer and floating-point computation.

**References**

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